

ABSTRACT OF THE DISCLOSURE

A semiconductor memory device with a built-in self test circuit includes a semiconductor substrate, a memory cell array formed on the semiconductor substrate, an input buffer provided on the semiconductor substrate to receive externally applied data, a test circuit coupled to the memory cell array and the input buffer on the semiconductor substrate to store a program received through the input buffer to generate test data of the memory cell array according to the stored program to carry out testing of the memory cell array, and a select circuit selectively applying to the memory cell array test data applied from the test circuit and data applied from the input buffer depending upon a test operation and a normal operation.

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